and a first semiconductor layer doped with an impurity and interposed between the active region and the metal-containing layer; and

a material layer which is interposed between the junction and the active region to prevent diffusion of the impurity from the first semiconductor layer and defines an opening for coupling the junction to the active region.

2. The electronic device of claim **1**, wherein a top surface of the first semiconductor layer is lower than a top surface of the gate.

3. The electronic device of claim **1**, wherein a thickness of the first semiconductor layer is smaller than a thickness of the metal-containing layer.

4. The electronic device of claim **1**, wherein the material layer includes a material which applies a stress to a channel of the transistor.

5. The electronic device of claim **1**, the material layer includes a silicon nitride.

6. The electronic device of claim **1**, further comprising:

a metal-semiconductor compound layer interposed between the first semiconductor layer and the metal-containing layer.

7. The electronic device of claim **1**, further comprising:

a second semiconductor layer which is formed in the opening and is positioned at a same level as the material layer in a vertical direction.

8. The electronic device of claim **7**, wherein the second semiconductor layer is an epitaxial semiconductor layer.

9. The electronic device of claim **7**, wherein a concentration of the impurity of the first semiconductor layer is higher than that of the second semiconductor layer or the active region.

10. The electronic device of claim **1**, a top surface of the active region is higher than a top surface of the isolation layer in a region where the gate is formed.

11. The electronic device of claim **1**, further comprising:

a memory element which is coupled to the junction disposed at one side of the gate.

12. The electronic device of claim **11**, wherein the memory element includes a variable resistance element which is switched between different resistance states according to an applied voltage or current.

13. The electronic device of claim **12**, wherein the variable resistance element includes a first magnetic layer, a second magnetic layer and a tunnel barrier layer interposed between the first magnetic layer and the second magnetic layer.

14. The electronic device according to claim **1**, further comprising a processor which includes:

a core unit configured to perform, based on a command inputted from an outside of the processor, an operation corresponding to the command, by using data;

a cache memory unit configured to store data for performing the operation, data corresponding to a result of performing the operation, or an address of data for which the operation is performed; and

a bus interface connected between the core unit and the cache memory unit, and configured to transmit data between the core unit and the cache memory unit,

wherein the transistor is part of at least one of the core unit, the cache memory unit and the bus interface in the processor.

15. The electronic device according to claim **1**, further comprising a processing system which includes:

a processor configured to decode a command received by the processor and control an operation for information based on a result of decoding the command;

an auxiliary memory device configured to store a program for decoding the command and the information;

a main memory device configured to call and store the program and the information from the auxiliary memory device such that the processor can perform the operation using the program and the information when executing the program; and

an interface device configured to perform communication between at least one of the processor, the auxiliary memory device and the main memory device and the outside,

wherein the transistor is part of at least one of the processor, the auxiliary memory device, the main memory device and the interface device in the processing system.

16. An electronic device comprising:

a substrate having an active region defined by an isolation layer;

a gate formed over the active region;

junctions formed on the active region and at both sides of the gate, each junction including a stack structure including an impurity doped semiconductor pattern and a metal-containing layer, wherein the concentration of an impurity of the impurity doped semiconductor pattern changes a resistance of an interface between the substrate and the junctions;

a diffusion barrier layer formed between the active region and the junctions to reduce diffusion of the impurity from the impurity doped semiconductor pattern, the diffusion barrier layer having a structure to apply a stress that increases mobility of charge carriers in a channel formed between the junctions.

17. The electronic device of claim **16**, wherein the metal-containing layer occupies the greater part of the junction.

18. The electronic device of claim **16**, wherein the impurity doped semiconductor pattern is positioned lower than the top surface of the gate.

19. The electronic device of claim **16**, further comprising:

an opening part formed between the active region and the junctions to electrically couple the active region with the junctions.

20. The electronic device of claim **16**, further comprising:

a memory element for storing data formed on the substrate and coupled to one of the junctions.

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